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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,627	08/29/2003	Kyoji Marumoto	12844.0040US01	1833
23552	7590	01/25/2006	EXAMINER	
MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903			PHAM, TAMMY T	
			ART UNIT	PAPER NUMBER
			2675	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/652,627

Applicant(s)

MARUMOTO, KYOJI

Examiner

Tammy Pham

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte. Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) and Yamamoto et al. (US Patent Application No: 2002/0140685 A1).

As for claim 1, AAPA teaches of an image display system comprising:  
a display memory for storing display image data to be displayed on a display panel;  
a CPU which is couple to the display memory and to the area image data generating section so as to perform controls thereof

wherein the CPU stores a frame image data to be a frame image into the display memory before the area image data is transferred to the display memory, whereby the frame image data and the area image data are composed with each other to form an image captured image data to be stored into the display memory, the in-frame captured image data being displayed on the display panel in section [0004].

The AAPA does not teach of an area image data generating section.

Yamamoto teaches of an area image data generating section (Yamamoto 24) for supplying an area image data which is corresponding to a specific area of a captured image data by an image capturing device (Yamamoto 12) to the display memory (Yamamoto 8) in section [0048].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the area image data generating section of Yamamoto with the image display system of the AAPA in order to save power through the image refreshing methods (see Yamamoto: section [0012]).

As for claim 2, AAPA teaches of a display device comprising:

A display panel;

A display memory for storing a display image data to be displayed on a display panel;

Storing means for storing a frame image data to be frame image to be supplied to the display memory in section [0005].

AAPA goes on to teach of an image capturing device;

A CPU which is connected to the display panel, the display memory, the storing means, the image capturing device;

Wherein the CPU reads out a frame image data to be a frame image from the storing means and stores the frame image data into the display memory before the image data is transferred to the display memory, whereby the frame image data and the area image data area composed with each other to form an in-frame captured image data to be stored into the display

memory, the in-frame captured image data being displayed on the display panel in section [0004].

The AAPA does not teach of an area image data generating section.

Yamamoto teaches of an area image data generating section (Yamamoto 24) for supplying an area image data which is corresponding to a specific area of a captured image data by an image capturing device (Yamamoto 12) to the display memory (Yamamoto 8) in section [0048].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the area image data generating section of Yamamoto with the image display system of the AAPA in order to save power through the image refreshing methods (see Yamamoto: section [0012]).

As for claim 3, Yamamoto teaches of a display device (Yamamoto Fig. 1) according to claim 2, wherein the area image data generating section (Yamamoto 24) includes a buffer memory (Yamamoto 16, 20) for storing the captured image data, specific area storing means (Yamamoto 15, 19) for storing the specific area in the captured image, and a transfer address generating circuit (Yamamoto 17, 21) for successively generating addresses of the specific area in the specific area storing means, wherein the addresses of the specific area generated by the transfer address generating circuit (Yamamoto 17, 21) are also supplied to the buffer memory (Yamamoto 16) so that an image data specified by the addresses are successively read out and output in section [0048].

As for claim 4, Yamamoto teaches of a display device (Fig. 1) according to claim 2, wherein the area image data generating section (Yamamoto 24) supplies to the display memory with the area image data corresponding to the specific area as a valid data, while an image data other than the specific area is defined as an invalid data in section [0015].

As for claim 5, Yamamoto teaches of a display device (Fig. 1) according to claim 4, wherein the area image data generating section (Yamamoto 24) includes a buffer memory (Yamamoto 16, 20) for storing the captured image data, specific area storing means (Yamamoto 15, 19) for storing the specific area in the captured image, gate means for receiving a gate signal from the specific area storing means, and a read-out address generating circuit (Yamamoto 17, 21) for generating a read-out address and supplying the read-out address to the buffer memory and the gate means (Yamamoto 16, 20), wherein only the read-out address corresponding to the specific area stored in the specific area storing means (Yamamoto 15, 19) is passed through the gate means so that the area image data is made valid, while the image data other than the area image data is made invalid in section [0015].

As for claim 6, Yamamoto teaches of a display device (Fig. 1) according to claim 3, wherein said specific area storing means (Yamamoto 15, 19) includes an area memory for storing the specific area as an area map in section [0048].

As for claim 7, Yamamoto teaches of a display device (Fig. 1) according to claim 3, wherein the specific area storing means (Yamamoto 15, 29) includes an area register used for

determining the specific area in accordance with the coordinates for plurality of points in section [0005, 0048].

As for claim 8, Yamamoto teaches of a display device (Fig. 1) according to claim 5, wherein the specific area storing means (Yamamoto 15, 19) includes an area memory for storing the specific area as an area map, and the read-out address generating circuit includes an area register used for determining a specific area for generating a read-out address in accordance with the coordinates for a plurality of points in section [0051].


### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2675

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Tammy Pham  
January 10, 2006

  
**KENT CHANG**  
**PRIMARY EXAMINER**